WHAT IS CLAIMED IS:

1. A structure of non-volatile memory, comprising:

a substrate;

a plurality of bit lines formed in the substrate along a first direction, wherein each of the bit lines also serve as a source/drain (S/D) region;

a first dielectric layer, disposed over the substrate;

a plurality of selection gate (SG) lines formed over the first dielectric layer between the bit lines;

a plurality of charge-storage structure layer, formed over the substrate between the bit lines and the SG lines;

a second dielectric layer, formed over the SG lines;

a third dielectric layer, formed over the bit lines; and

a plurality of word lines, formed over the substrate along a second direction, which is crossing the first direction for the bit lines.

2. The structure of non-volatile memory of claim 1, wherein the charge-storage structure layer includes a charge-trapping dielectric layer.

3. The structure of non-volatile memory of claim 2, wherein the charge-trapping dielectric layer at the region above the bit lines is discontinuous or continuous.

4. The structure of non-volatile memory of claim 2, wherein the charge-trapping dielectric layer includes a horizontal part over the substrate and a vertical part over sidewall of the SG lines.

5. The structure of nonvolatile memory of claim 4, wherein the charge-trapping dielectric layer further comprises another horizontal part over the second dielectric layer.

6. The structure of non-volatile memory of claim 1, wherein the charge-storage structure layers includes a floating gate layer for charge storage.

7. The structure of non-volatile memory of claim 1, further comprising:

a plurality of bank-select transistors respectively disposed between the S/D regions and the bit line voltages for selection and applying the bit line voltage.

8. The structure of non-volatile memory of claim 1, further comprising a source voltage supplying structure coupled to the SG lines, so that a desired voltage state is applied to the selected one of the memory cells to form an operation path.

9. A structure of a non-volatile memory unit with two-bit memory capacity, comprising:

a substrate;

two doped lines, located in the substrate;

a selection gate structure line, disposed on the substrate between the two doped lines;

a charged storage structure layer, located each side of the selection gate structure line between the doped lines and the selection gate line;

a first dielectric layer, disposed over the selection gate structure line;

a second dielectric layer, disposed over the doped lines; and

a gate electrode layer, disposed crossing over the doped lines and the selection gate structure line.

10. The structure of claim 9, wherein the charged storage structure layer comprises a dielectric/charge-storage/dielectric structure layer or a floating gate structure layer.

11. The structure of claim 10, wherein the charged storage structure layer

comprises an oxide/nitride/oxide structure layer.

12. A circuit layout for a non-volatile memory device, comprising:

a plurality of MOS memory cells, arranged into rows and columns, wherein each of the MOS memory cells has two charge storage nodes commonly coupled with one selection gate (SG) line corresponding to the columns;

a plurality of buried bit lines coupled between adjacent two of the memory cells, to also serve as S/D electrodes of the memory cells;

a plurality of word lines, coupled to the memory cells with respect to the rows, also serve as gate electrodes of memory cells; and

a first and a second SG voltage feeding lines, wherein the SG lines are alternatively coupled to the first and the second SG voltage feeding lines,

wherein when the first SG voltage feeding line or the second SG voltage feeding line is applied with a activating voltage, a created S/D region occurs between the two charge storage nodes, so that a proper source voltage can be applied to the created S/D region to operate with the S/D electrode from the bit lines.

13. The circuit layout of claim 12, wherein bank-select transistors are coupled between the bit lines and bit line voltage sources.

14. The circuit layout of claim 12, wherein when a memory cell is selected, the SG line related to the selected memory cell is applied with the activating voltage while the adjacent SG line for the adjacent cells are set to a ground voltage.

15. The circuit layout of claim 14, wherein all of the created S/D regions are coupled to a source voltage.

16. The circuit layout of claim 14, wherein each of the first and the second SG voltage feeding lines is coupled to a gate electrode of a MOS transistor, and the MOS

transistor has a first S/D electrode coupled to a source voltage, and a second S/D electrode coupled to all of the created S/D regions.

17. The circuit layout of claim 14, wherein all of the created S/D regions are floating.

18. The circuit layout of claim 14, wherein every two adjacent created S/D regions are grouped as one and coupled to a source voltage.

19. The circuit layout of claim 14, wherein every four adjacent created S/D regions are grouped as one and coupled to a source voltage.

20. A circuit layout for a non-volatile memory device, comprising:

a plurality of MOS memory cells, arranged into rows and columns, wherein each of the MOS memory cells has two charge storage nodes commonly coupled with one selection gate (SG) line corresponding to the columns;

a plurality of buried bit lines coupled between adjacent two of the memory cells, to also serve as S/D electrodes of the memory cells;

a plurality of word lines, coupled to the memory cells with respect to the rows, also serve as gate electrodes of memory cells; and

at least three SG voltage feeding lines, wherein the SG lines are alternatively coupled to the SG voltage feeding lines,

wherein three adjacent SG lines controlled by the SG voltage feeding lines are operated together to prevent a leakage to the adjacent memory cell, and when one of the SG voltage feeding lines is applied with a activating voltage, a created S/D region occurs between the two charge storage nodes.

21. The circuit layout of claim 20, wherein the at least three SG voltage feeding lines is three SG voltage feeding lines, and one of the SG voltage feeding lines

corresponding to the selected one of the memory cells is at the activating voltage while the other two are at ground voltage.

22. The circuit layout of claim 21, wherein the unselected adjacent bit lines are set to a floating state.